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Lateral diffusion properties of arsenic.in polycrystalline silicon.

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LATERAL DIFFUSION PROPERTIES OF ARSENIC IN POLYCRYSTALLINE SILICON

by

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October 16, 1979
Date

Professor in Charge

Chairman of the Department

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TABLE OF CONTENTS

	Page
List of Tables	vi
List of Figures	vii
Abstract	1
1.0 Introduction	3
2.0 Experimental Procedure	4
2.1 Resistor Geometry	4
2.2 Test Pattern	5
2.3 Sample Preparation	6
2.4 Four Cell Experiment	8
2.4.1 Arsenic - Ion Implant	8
2.4.2 Arsenic - Emulsion Base	8
2.4.3 Phosphorus - Ion Implant	9
2.4.4 Phosphorus - Predeposition	9
3.0 Electrical Measurements	9
4.0 Experimental Results/Analysis/Discussion	10
4.1 Four Cell Experiment	10
4.1.1 Arsenic - Ion Implant	12
4.1.2 Arsenic - Emulsion Base	12
4.1.3 Phosphorus - Ion Implant	13
4.1.4 Phosphorus - Predeposition	13
4.2 Poly-Si Film Deposition	13

	Page
4.3 Activation Energy Calculation	14
4.4 Breakdown Voltage Versus R_L	16
4.5 Breakdown Voltabe Versus R_W	16
4.6 Model	17
4.7 Process Design Guide	18
5.0 Conclusions	21
Tables	22
Figures	24
References	38
Appendix 1	39
Vita	40

LIST OF TABLES

		Page
Table 1	Process Steps	22
Table 2	Deposition System/Ion Implant Dose Effects On R_L'	23

LIST OF FIGURES

		Page
Figure 1	Basic Flip-Flop Circuit	24
Figure 2	Basic Resistor Configuration	25
Figure 3	Test Pattern	26
Figure 4	Process Steps	27
Figure 5	Current - Voltage Characteristics	28
Figure 6	Arsenic - Ion Implant	29
Figure 7	Arsenic - Emulsion Base	30
Figure 8	Phosphorus - Ion Implant	31
Figure 9	Phosphorus - Predeposition	32
Figure 10	$2\Delta L$ Vs. Temperature^{-1}	33
Figure 11	Symbolic Representation of Impurity Diffusion Through Poly-Si	34
Figure 12	V_{BD} Vs. R_L	35
Figure 13	Breakdown Voltage Dependence on Resistor Width	36
Figure 14	A. I-V Curve B. Schematic C. Physical Model	37

ABSTRACT

It is desirable to have a high impedance circuit element which consumes a minimal amount of area for use in integrated circuits. In MOS technology, the use of undoped polycrystalline silicon (poly-Si) has been incorporated in recently designed static RAM's.[1,2]

The static RAM circuits are fabricated in a single level poly-Si MOS technology using arsenic as the poly-Si and source/drain impurity dopant. The diffusion of arsenic in poly-Si is expected to be enhanced when compared with single crystal silicon due to the occurrence of grain boundaries in the polycrystalline material. Early in the process development it was necessary to study the diffusion properties of arsenic in poly-Si films. This paper reports the data accumulated in an experiment which studied the lateral diffusion of arsenic in 0.5μ poly-Si films as a function of time, temperature, concentration and source of impurity. For comparative purposes, data was also generated for the lateral diffusion of phosphorus under similar conditions.

The data suggests a model for these resistors of back-to-back diodes with the reverse breakdown potential dependent upon its geometric properties. The breakdown mechanism appears to be an impact ionization phenomena.

An activation energy for the lateral diffusion of arsenic in poly-Si was calculated to be 3.4 eV. This compares of 4.2 eV for the diffusion of arsenic in single crystal silicon. Because the diffusion coefficient is exponentially dependent upon the activation energy the 0.8 eV difference accounts for the enhanced diffusion rate of arsenic in poly-Si.

The diffusion rate of both arsenic and phosphorus is directly dependent upon its initial concentration and essentially independent of its source. Also, for ion implantation of either arsenic or phosphorus of equal sheet resistances the diffusion rates are similar.

Based on the data presented, design size considerations for resistor length may be extracted from a knowledge of the heat treatment cycle.

1.0 INTRODUCTION

In the fabrication of certain integrated circuits it is necessary to construct a circuit element using a minimal amount of area, which provides a non-critical, high value impedance, i.e., > 10 MΩ. An example of its application is in a flip-flop circuit as shown in Figure 1. Here one side of the circuit is held at power supply potential via the resistive path in this cross coupled circuit. To be economical in the area consumed by the resistive component, the use of undoped polycrystalline silicon (poly-Si) can be employed. Physically the resistor would be a length of undoped poly-Si with doped ends for contacts.

Present fine line design rules used in today's integrated circuit designs necessitates the use of slow diffusers for processing. In MOS technology, arsenic is most often the choice. The diffusion of arsenic in single crystal silicon is well understood.[3,4] It is expected that the diffusion in poly-Si would be enhanced due to its grain boundaries.

Recent designs of 4K static RAM's utilized a flip-flop circuit for the memory storage element. The circuits are fabricated using an improved single poly-Si MOS technology[5] which uses arsenic for doping the

source/drain regions and the poly-Si. An important consideration in the fabrication of these resistors is the lateral diffusion of the dopant with time and temperature. This paper empirically studies the lateral movement of arsenic in poly-Si films in the order of 0.5 μm thick. The dependency of the source of arsenic is investigated. Also, phosphorus, another commonly used dopant in MOS processing, is studied for comparison.

2.0 EXPERIMENTAL PROCEDURE

2.1 Resistor Geometry

In its simplest form a high impedance resistor configuration using undoped poly-Si would be as shown in Figure 2. The resistor width (R_W) is defined by a strip of poly-Si and the resistor length (R_L) is defined by the size of the silicon dioxide (SiO_2) strip. The purpose of the SiO_2 is to mask impurity doping in the center of the structure. In a workable MOS technology the resistor width would be patterned in poly-Si at the same time as the transistor gates. The transistor length would then be patterned via a SiO_2 masking level and the structure would then be exposed to an impurity dopant, creating the n^+ regions. The resistor ends would be doped and, therefore, ohmic

contact would be made to them. But, the center of the component would not be doped by virtue of the SiO_2 masking oxide. It is possible and convenient to dope the resistor ends while the source and drain regions of the transistors are doped. Thereafter, the lateral movement or underdiffusion (ΔL) of arsenic would be due to subsequent heat treatments in the process.

In order to determine the lateral movement of arsenic and phosphorus in poly-Si, a test pattern was fabricated which had various feature sizes. With this pattern the lateral diffusion could be quantitatively measured. Minimum size design information can be retrieved from the data.

2.2 Test Pattern

A test pattern, which was initially designed to study various NMOS transistor geometries, was used to make the resistor test patterns. A photograph of the test pattern is shown in Figure 3. The top of the figure shows the entire chip and the bottom has a blown-up view showing the varying line widths. The pattern provides an array of transistors varying in device width and channel length from 1 μm to 50 μm. Therefore, for a device width of 50 μm, channel lengths ranged from 1 μm

to 50 μm. Dimensions in both directions were stepped in 0.5 μm steps below 10 μm and 1 μm steps between 10 μm to 20 μm, then steps of 5 μm were used. To fabricate the resistors for this experiment a simple mask assignment change was made. The mask which normally defines the transistor width was used to define the resistor strip in poly-Si. And, the mask which normally serves as the transistor channel length (gate mask) was used to define the resistor length in the SiO_2 masking oxide.

The test pattern also contained a feature to obtain the diffused sheet resistance value of the poly-Si films.

2.3 Sample Preparation

The resistors were prepared using an abbreviated MOS type process performing only the significant steps needed to form the resistors. Table 1 lists the process steps which were followed and Figure 4 shows cross-sectional views throughout the fabricational sequence. The wafers were cleaned and 7,000Å of SiO_2 was grown. Next, a 6,000Å poly-Si film was deposited (Figure 4A). Next, a sacrificial oxide was grown. A photoresist step follows

which defines the resistor width. This photoresist pattern is next defined in the underlying oxide by means of an oxide etch. Because the photoresist will not hold up in the poly-Si etchant it must be removed, and now the oxide pattern will serve as the etch mask. At this point the poly-Si was etched in a chromic/hydrofluoric acid solution defining the resistor width (Figure 4B). The sacrificial oxide was removed next and the wafers cleaned. Then, 2,000Å of SiO_2 was grown on the poly-Si prior to a SiO_2 film deposition of 5,000Å (Figure 4C). The deposited oxide is annealed prior to a photoresist step and an oxide etch which defines the impurity mask or the resistor length in the deposited SiO_2 film (Figure 4D). This serves as a dopant barrier for the next step which was a four cell processing variable in this study (Figure 4E). Next, the ion implanted samples received a 900°C, 60 minute nitrogen anneal while the predeposited samples received a reoxidation step of 800°C steam oxide for 25 minutes. Finally, the samples were given a 1,000°C dry oxygen heat treatment for varying times from 10 minutes to 80 minutes. The final

cross-sectional structure is shown in Figure 4F showing R_L, ΔL, and n^+ regions.

2.4 Four Cell Experiment

The primary concern was to derive information regarding the lateral movement of arsenic in poly-Si. In order to achieve this and also provide a broader background, an experiment which had four major cells was performed. Two of the cells used arsenic as an impurity and two used another commonly used impurity, phosphorus. Each of these were further subdivided to investigate the dependency upon the source of the impurity. The arsenic was; 1) ion implanted and 2) spun on using an emulsion base carrier. The phosphorus was; 1) ion implanted and 2) applied in a diffusion furnace.

2.4.1 Arsenic - Ion Implant

Test samples were prepared using ion implantation of arsenic at an energy of 30 KeV. Four different doses were implanted into the wafers of 1×10^{15} a/cm^2, 2×10^{15} a/cm^2, 5×10^{15} a/cm^2, and 1×10^{16} a/cm^2.

2.4.2 Arsenic - Emulsion Base

A commercially available emulsion coating containing arsenic was applied to samples for evaluation.[6] The substance is applied much

like a spun-on photoresist coating. Included in the application procedure is an initial heat treatment of 1,000°C 50/50 mixture of oxygen and nitrogen for 30 minutes.

2.4.3 Phosphorus - Ion Implant

Samples were fabricated with phosphorus ion implantation using identical energies and doses as the arsenic implanted samples.

2.4.4 Phosphorus - Predeposition

Samples were prepared in PBr_3 diffusion furnaces for 30 minutes. Two different temperatures were studied; namely, 900°C and 950°C.

3.0 ELECTRICAL MEASUREMENTS

To determine how the various dopants diffused laterally with time and temperature in the poly-Si films, current versus voltage (I-V) measurements were made. Electrical contact from the measurement probes to the test devices was made directly to the doped poly-Si resistor ends. To compare the four cell experiment, data was taken by measuring the various resistor lengths. The data was taken for R_W equal to 50 μm.

Figure 5 is a series of plots showing oscilloscope tracings of typical I-V characteristics for various resistor lengths. If the resistor length is very narrow,

the underdiffusion of the impurity is such that the ends "short" together, yielding a low value resistor as seen in Figure 5A. As the resistor lengthens, a non-linear shape occurs as shown in Figure 5B. For successively larger lengths, the I-V curves generated are as shown in Figures 5C, 5D, and 5E. (Note the scale changes on the voltage axis.) As can be seen, the larger resistor lengths exhibit a back-to-back diode characteristic with its reverse breakdown voltage becoming larger for increases in R_L.

4.0 EXPERIMENTAL RESULTS/ANALYSIS/DISCUSSION

4.1 Four Cell Experiment

To compare the lateral diffusion property of the various processing cells, all the samples were measured to determine the value of R_L which produced the same breakdown voltage. The breakdown mechanism appears to be an impact ionization effect. The value of breakdown potential increases as the distance between the doped resistor ends defined by the resistor length (R_L) is made larger. A breakdown voltage V_{BD} range between 10V to 18V was chosen as a reference. This range was selected based on the fact that during the measurements a 15V breakdown increase is observed for every 1 μm increase

in resistor length. This makes the measurements accurate to 0.5μ in resistor length or 0.25μ in diffusion distance.

The data presented in this section is plotted so that the various processing cells can be compared. The curves show how the underdiffusion of the impurity is effected by heat treatment.

The ordinate is calibrated in μm and represents the lateral diffusion of the impurity. To determine the lateral diffusion of the impurity from the R_L measurement, the following was considered. A critical resistor length (R_L') was defined to compare the processing variations, which corresponds to two times the underdiffusion of the impurity plus the distance between the impurity edges maintaining an ionization potential between 10V to 18V. Two times the underdiffusion of the impurity is the total distance traveled by the impurity, and the distance between the impurity edges is the region of undoped poly-Si. Expressing this in equation form:

$$R_L' = 2\Delta L + X \qquad (1)$$

where:

R_L' = resistor length yielding 10V to 18V breakdown range,

ΔL = underdiffusion of impurity, and

X = distance maintaining ionization potential from 10V to 18V.

As mentioned earlier, a 15V breakdown change is noted for a change in R_L' of 1 μm. Therefore, to approximate ΔL using Equation (1), set X = 1.0 μm and measure R_L' yielding 10V to 18V breakdown, then ΔL can easily be determined.

The abscissa for the curves in this section is expressed in minutes and is a measure of the drive-in time at 1,000°C dry oxygen for which the samples were exposed.

4.1.1 Arsenic - Ion Implant

Figure 6 shows the family of curves received for the different doses of arsenic ion implant. This reflects a sheet resistance of the poly-Si ranging from 75 Ω/□ to 1,500 Ω/□. Depending on this and the time-temperature treatment, ΔL ranged from 0.25 μm to 3 μm.

4.1.2 Arsenic - Emulsion Base

From the processing described in a previous section, a sheet resistance of 175 Ω/□

was obtained. Figure 7 shows the probe results of underdiffusion (ΔL) versus drive-in time for this cell of the experiment.

4.1.3 Phosphorus - Ion Implant

The family of ΔL versus drive-in time curves for the phosphorus implant samples is shown in Figure 8. Identical energy of implant and doses were used as for the arsenic implanted samples. Sheet resistance ranged from 30 $\Omega/\square$ to 600 $\Omega/\square$ for the different doses, with ΔL changing from approximately 0.1 μm to 3.5 μm, depending on time/temperature.

4.1.4 Phosphorus - Predeposition

The probe results showing ΔL versus drive-in time for the two predeposition temperatures are plotted in Figure 9. The upper and lower curves are for 950°C (30 $\Omega/\square$) and 900°C (50 $\Omega/\square$) temperature, respectively.

4.2 Poly-Si Film Deposition

To explore whether there are any differences in the poly-Si films due to the deposition system which might alter the lateral diffusion property of an impurity, a group of wafers had the poly-Si deposited in three different in-house reactors. The table shown below describes the available systems:

Manufacturer	Pressure	% Silane	Temperature (°C)
Applied Material Technology	LP-CVD	17	600
Nitrox	ATM.	15	765
Tempress-Unicorp	LP-CVD	100	600

These wafers were subsequently split in ion implant dose and drive-in time for the primary part of the experiment. Table 2 lists the R_L data for the various splits. By comparing R_L for the different doses and drive-in times against the deposition systems, it can be seen that no significant differences between deposition systems occur. This implies that the films are essentially equivalent after annealing and other processing heat treatments.

4.3 Activation Energy Calculation

A calculation of the lateral diffusion activation energy of arsenic in poly-Si was performed (see Appendix 1 for details). The plot of $2\Delta L = (R_L' - X)$, where $X = 1\mu$, versus temperature is shown in Figure 10. From the slope of this curve and considering Equation (2),

$$D = D_o\, e^{-E/kT} \qquad (2)$$

an activation energy of 3.4 eV was calculated. This is an 0.8 eV differential as compared to

published data of 4.2 eV[7] for the activation energy of arsenic in single crystal silicon. Considering the diffusion coefficient (D) is exponentially dependent on activation energy, this 0.8 eV in the 1,000°C temperature region accounts for a large increase in D.

The other term in Equation (2) is D_o, which can be determined from the y-axis intercept of Figure 10. Values for D_o depend on particulars of sample preparation such as impurity concentrations. A value of 660 cm^2/sec was calculated from the data presented here which compares to a value of 60 cm^2/sec for arsenic in single crystal silicon.[7]

For the purposes of this study the exact values calculated are not as important as the fact that both terms are in the direction to predict enhanced diffusion of arsenic in poly-Si films. These values are consistent with the theory that the impurity will diffuse along the grain boundaries more rapidly and then diffuse outward as it travels. This is depicted in Figure 11 by assuming a hexagonal grain structure for the poly-Si. The impurity diffuses

out from the grain boundaries at the bulk diffusion rate. The total effect is an enhanced diffusion in poly-Si as compared to single crystal silicon.

4.4 Breakdown Voltage Versus R_L

As the resistor length increases the breakdown voltage increases. Figure 12 is a plot showing this relationship. Three different doses of ion implanted arsenic (1×10^{15}, 2×10^{15}, and 1×10^{16} a/cm^2), each for three different drive-in times (10, 20, and 80 minutes), were measured. The important point derived from these curves is that all the slopes were in a tight range of 13V/μm to 17V/μm. This is one of the reasons the 10V to 18V voltage range was chosen to generate the earlier data.

4.5 Breakdown Voltage Versus R_W

It was observed that a short width effect exists for these devices. The property is that for a given resistor length, R_L; as smaller widths were measured, the effective X was reduced.

Figure 13 is a plot showing this phenomenon for both arsenic and phosphorus ion implanted samples and phosphorus predeposited samples. This is a normalized plot which shows the deviation of the breakdown voltage from that which was measured for a 50 μm width

device. For R_W below 10 μm, the effective resistor length becomes smaller. The ion implanted samples show only a minor effect. This corresponds to an effective resistor length change of 0.5 μm. For the phosphorus predeposited samples the effect is much more noticeable and corresponds to a 4 μm effective change in X below 10 μm in R_W.

4.6 Model

The symmetrical I-V characteristic observed on a μa scale (Figure 14A) suggests a model of back-to-back diodes with a high value resistor between them (Figure 14B). A top view of the physical resistor is again shown in Figure 14C. The value of resistance in the model is determined by the center intrinsic region. This value of resistance when examined on a more microscopic basis[8] is probably due to the poly-Si band gap structure having various defect sites giving rise to leakage current. The diodes D1 and D2 are generated by the intrinsic/n^+ junctions formed by doping the resistor ends while the center portion is masked. This effective junction is shown in Figure 14C by the dashed line. The distance between the two dashed lines is called $R_{L(EFF)}$, and in the special case of maintaining

a 10V to 18V breakdown is called X. Also shown is ΔL, the underdiffusion of the impurity.

The breakdown potential is dependent on the resistor length as shown in Figure 12. This breakdown phenomena appears to be an impact ionization or avalanche effect when the applied field is strong enough. The average slope of all the V_{BD} versus R_L curves is approximately 15V/1 μm. This is within a factor of two to the published data on the ionization potential for single crystal silicon of ∿ 30V/μm.[9] The difference observed may be due to the high leakage currents in poly-Si films.

An expression for the breakdown point is:

$$V_{BD} = \alpha\ (R_L - 2\Delta L) \qquad (3)$$

where $\alpha = 15V/\mu m$.

4.7 Process Design Guide

Considering the experimental results presented leads to the following conclusions. First, as the sheet resistance decreases, an increase in resistor length is necessary to obtain the same breakdown voltage. For example, referring to Figure 6, a 60 minute dry oxygen drive-in time results in underdiffusions of about 0.5 μm and 2.5 μm for the respective sheet resistances of 1,500 Ω/□ and 75 Ω/□.

This may be explained as an impurity concentration effect in that the lateral diffusion length is dependent upon the initial dopant level.

Second, the underdiffusion (ΔL) of the impurity does not have a strong dependency on the sources of the arsenic investigated here. This can be seen by comparing the two curves of Figures 6 and 7 at equal sheet resistances. The curves show the largest discrepancy at the shorter drive-in times; but, for longer times the curves are within 0.5 μm of each other. Considering the measurement category (10V to 18V) has a spread of 0.5 μm, the lateral diffusion is not effected greatly by the source of the arsenic impurity.

Third, comparing the sources of phosphorus chosen here (ion implantation and predeposition) an initial discrepancy in underdiffusion is observed which remains throughout the subsequent heat treatment. Comparing Figures 8 and 9 show that the predeposited samples possess greater ΔL than the ion implanted samples to produce an equivalent breakdown potential at a given drive-in time. This may be due to the predeposition temperature itself laterally diffusing the impurity farther than ion implantation.

Also noted is a noticeably steeper slope to the 950°C phosphorus predeposition (30 Ω/□) curve than the 1×10^{16} a/cm^2 (30 Ω/□) ion implanted phosphorus data.

Fourth, comparing the arsenic and phosphorus ion implanted samples shows that the data is essentially the same. This implies that the lateral diffusion of the two ion implanted impurities in poly-Si films of this thickness (0.50μ) are very similar.

Fifth, no discernible differences were noted in the diffusion of the impurity phosphorus for the various poly-Si films deposited from the three different in-house reactors.

Finally, based on the data presented, a minimum size device may be estimated to produce a functional high value resistor. This may be accomplished by singling out any given dopant and calculating an equivalent time at 1,000°C for a process to determine the maximum ΔL and, in turn, minimum R_L. For example, for 30 KeV energy ion implant of arsenic at 1×10^{16} a/cm^2 with an equivalent time at 1,000°C of 80 minutes a minimum R_L would equal 7μ. To increase the breakdown voltage point, an increase of 1 μm will yield a 15V jump.

5.0 CONCLUSIONS

Lateral diffusion properties of arsenic and phosphorus in 0.5μ thick poly-Si films were determined. Motivation for this study was to fabricate high impedence resistors in a small area. The data presented provides minimum design information.

Processing parameters of time-temperature, impurity concentration, source of impurity, and poly-Si were investigated. Both arsenic and phosphorus diffusion is directly dependent upon its concentration and essentially independent of its source. For equal sheet resistance of ion implanted arsenic and phosphorus, the diffusion properties are similar.

For the lateral diffusion of arsenic in poly-Si an activation energy of 3.4 eV was calculated. This is 0.8 eV lower than arsenic in single crystal silicon. The diffusion coefficient is exponentially dependent upon the activation energy and the difference accounts for the enhanced diffusion rate.

The data presented supports a model for these resistors of back-to-back diodes (n^+/intrinsic/n^+) with the reverse breakdown potential dependent upon its geometry. The breakdown mechanism appears to be an impact ionization effect.

TABLE 1

PROCESS STEPS

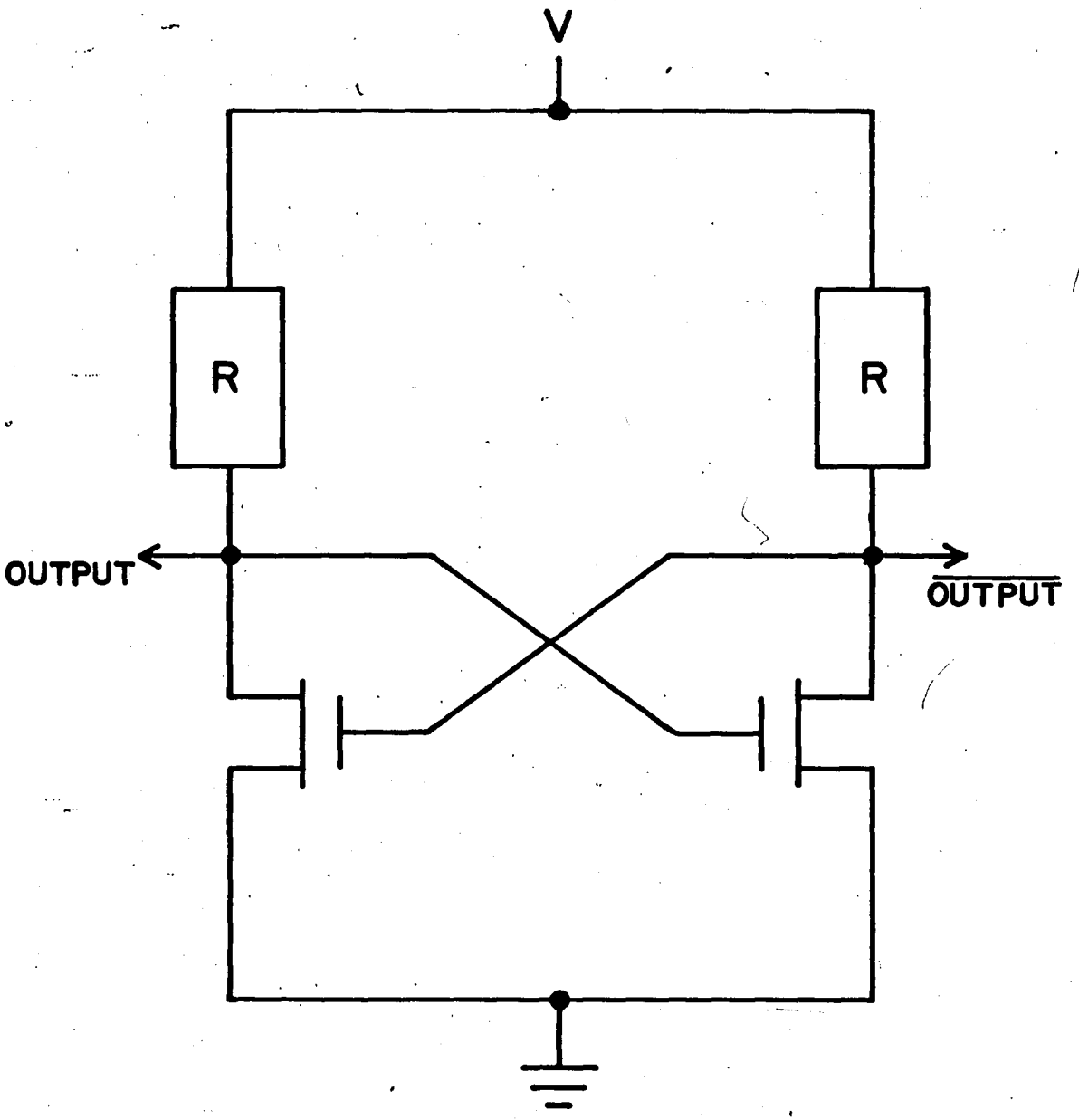
1. CLEAN
2. STEAM OXIDE - 1,000°C 200 MINUTES
3. DEPOSIT POLY-SI - 6,000Å
4. STEAM OXIDE - 950°C 35 MINUTES
5. PHOTORESIST RESISTOR WIDTH
6. OXIDE ETCH - BHF 3 MINUTES
7. RESIST STRIP J-100
8. CLEAN
9. POLY-SI ETCH - CRO_3/HF 4-1/2 MINUTES
10. OXIDE ETCH - BHF 1-1/2 MINUTES
11. CLEAN
12. DRY OXIDE - 1,000°C 60 MINUTES
13. DEPOSIT OXIDE 5,000Å
14. STEAM OXIDE - 1,000°C 30 MINUTES
15. PHOTORESIST RESISTOR LENGTH
16. OXIDE ETCH - BHF 7 MINUTES
17. RESIST STRIP J-100
18. CLEAN
19. DOPANT (FOUR CELL EXPERIMENT - 1) As - ION IMPLANT, 2) As - EMULSION BASE, 3) P - ION IMPLANT, AND 4) P - PREDEPOSITION)
20. CLEAN
21. NITROGEN ANNEAL - 900°C 60 MINUTES (ION IMPLANTED SAMPLES ONLY)
22. STEAM OXIDE - 800°C 25 MINUTES (PREDEPOSITED SAMPLES ONLY)
23. DRY OXIDE - 1,000°C (10 TO 80) MINUTES

TABLE 2

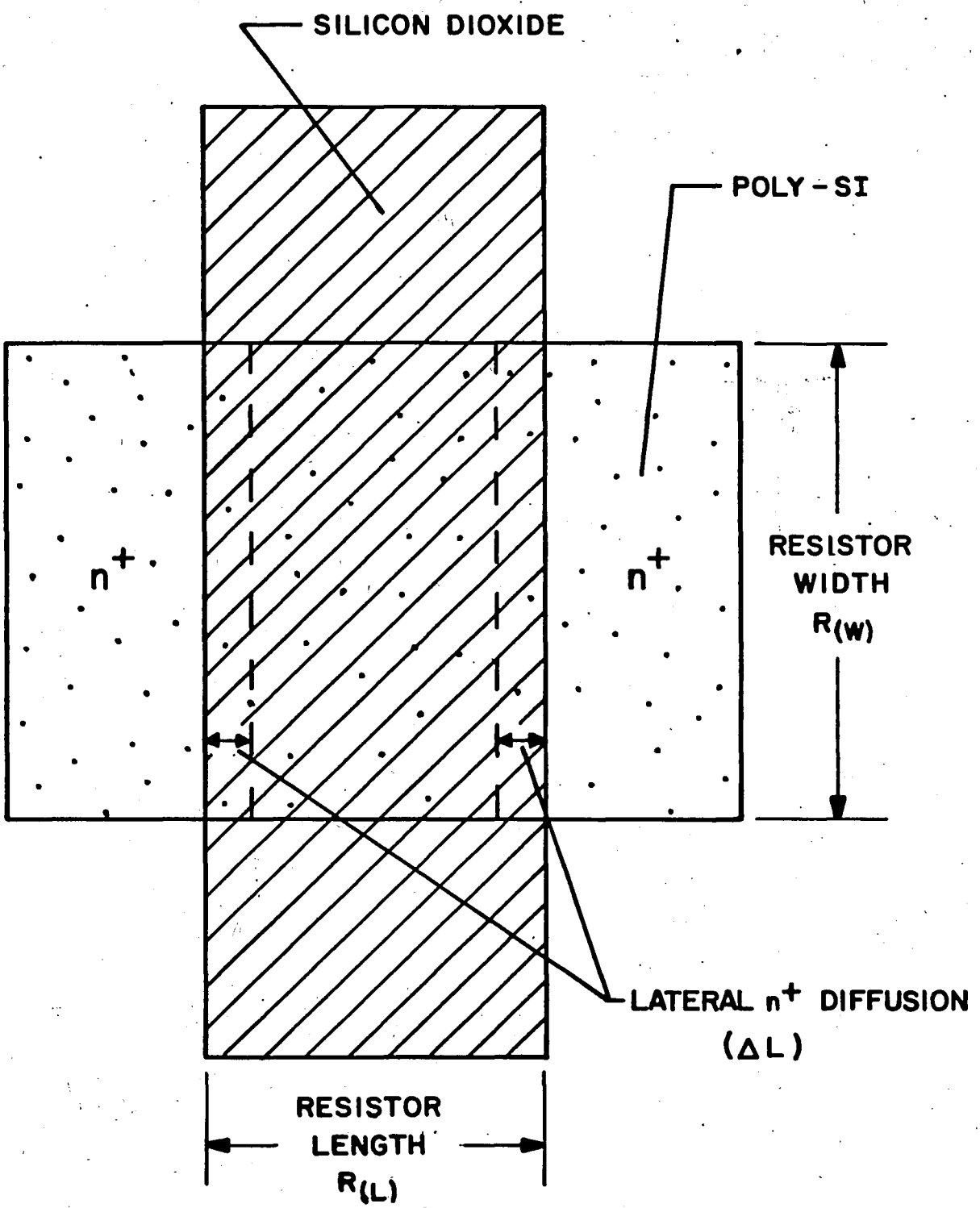
DEPOSITION SYSTEM/ION IMPLANT DOSE EFFECTS ON R_L'

Phos. Ion Implant 30 KeV x 10^{15}	Poly-Si Deposition System*	R_L' (μm) Drive-In Time At 1,000°C			
		10M	20M	40M	80M
10	N			7.0	9.0
	A	5.5	7.5		
	U			9.0	10.0
5	N	4.5	5.5		
	A			6.5+	8.0
	U	4.5	5.5		
2	N	4.0	4.5		
	A			5.5	6.5
	U			4.0	6.5
1	N	3.5	4.0		
	A			4.5	5.0
	U	3.5	4.0		

*N - Nitrox
A - Applied Material Technology
U - Tempress-Unicorp

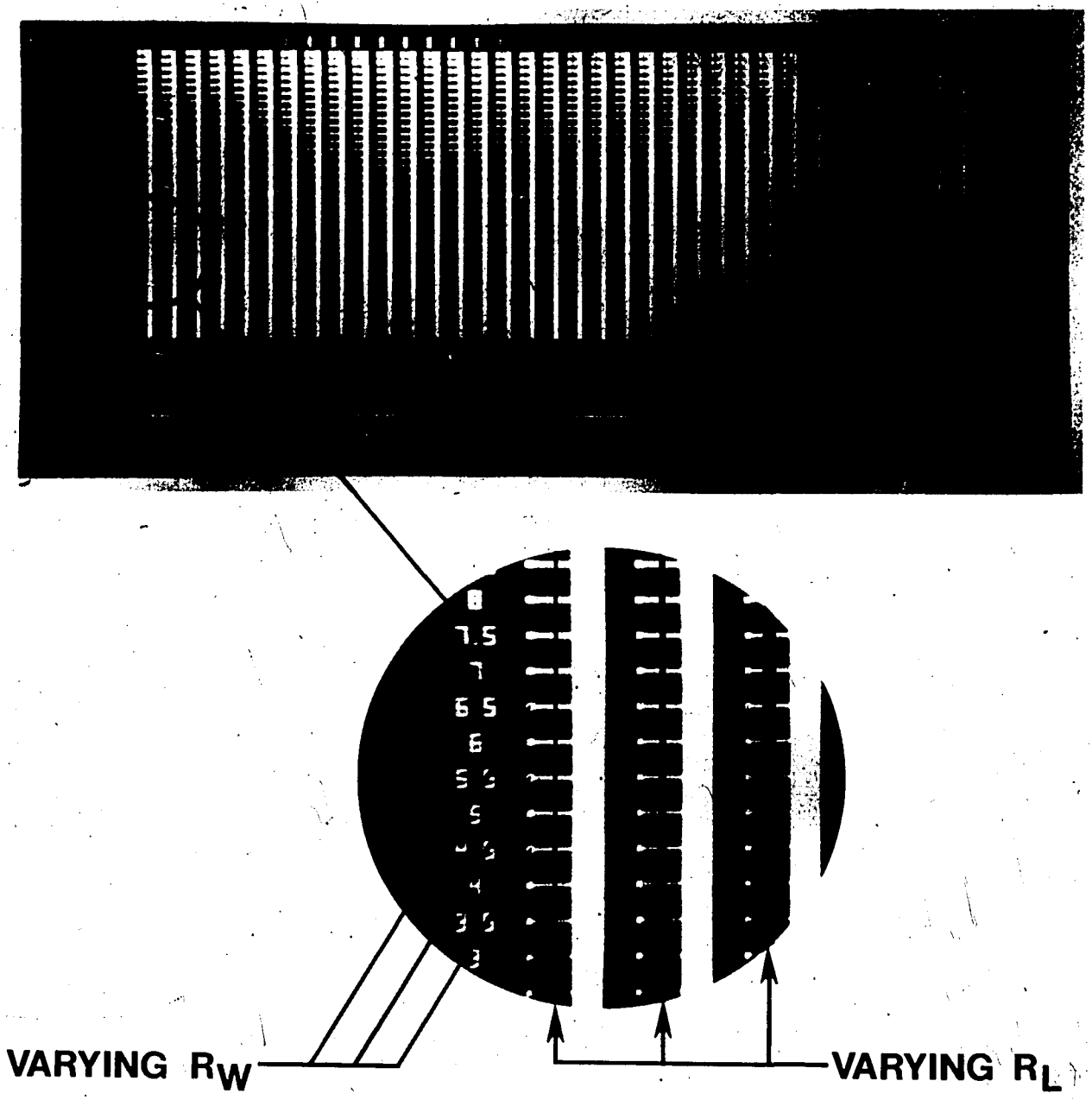


BASIC FLIP FLOP CIRCUIT
R=UNDOPED POLY-SI RESISTORS
FIGURE 1

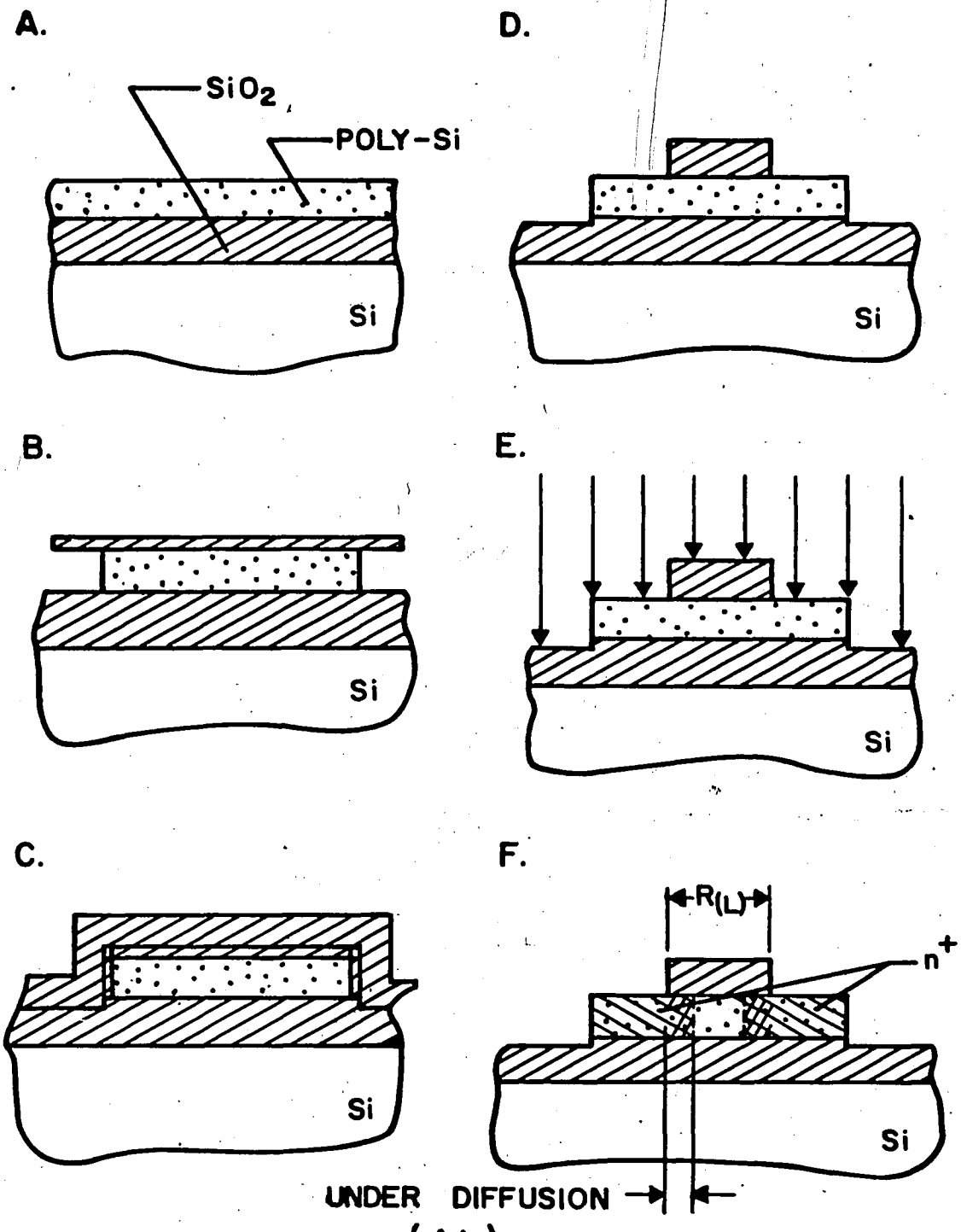


BASIC RESISTOR CONFIGURATION

FIGURE 2

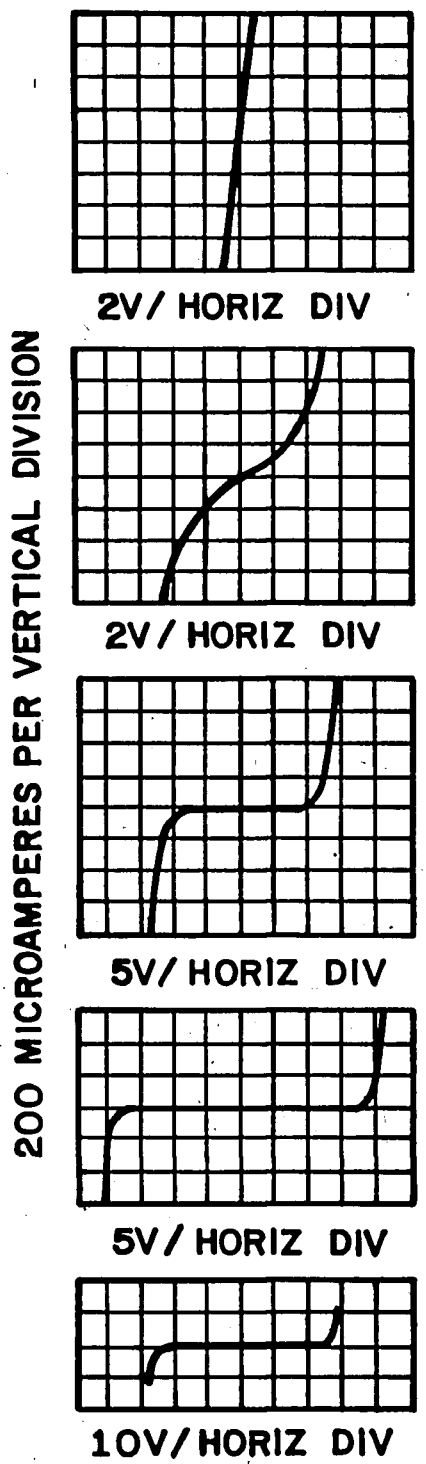


TEST PATTERN
FIGURE 3



PROCESS STEPS

FIGURE 4



A.
$R_L < 2(\Delta L)$

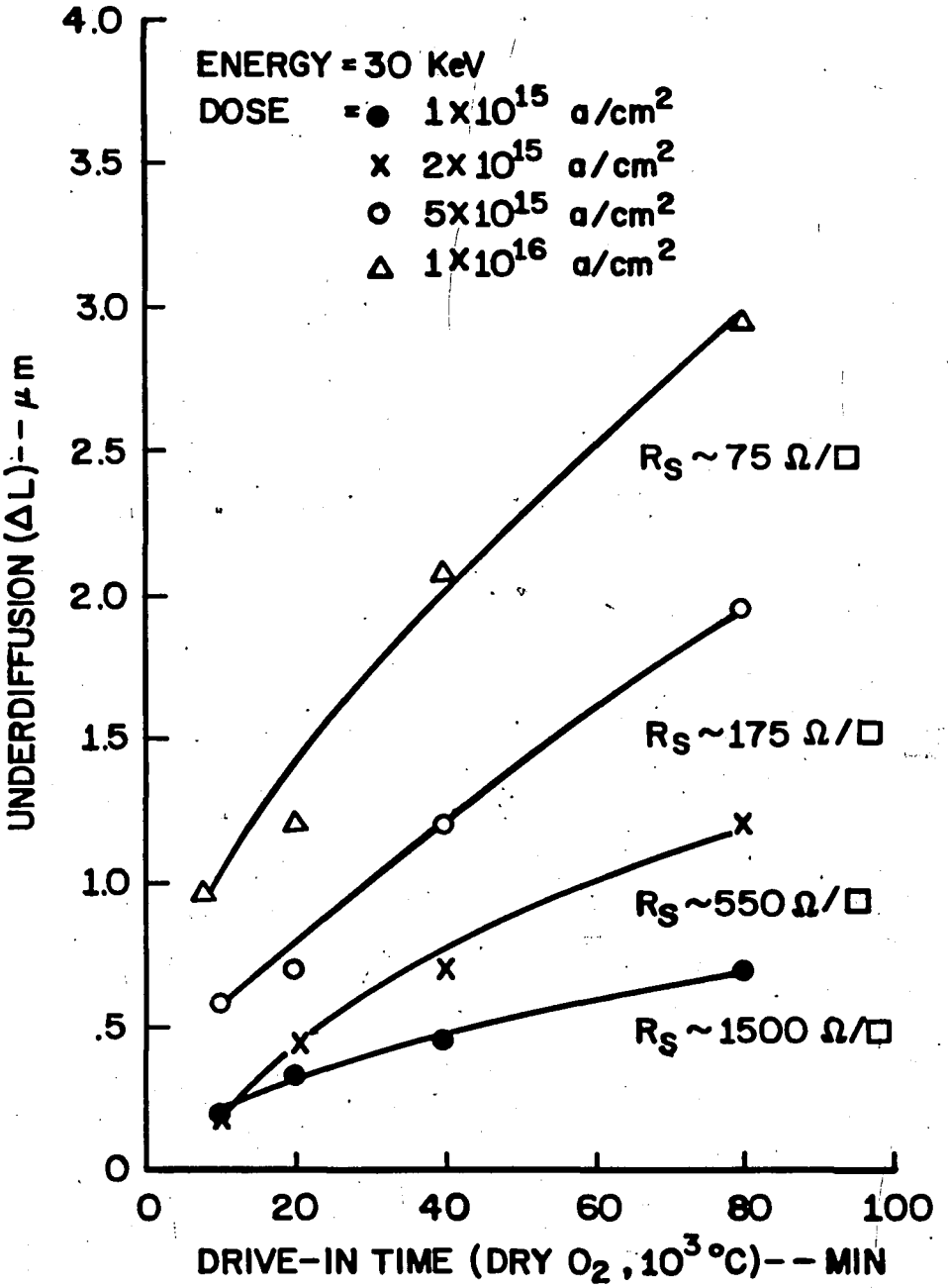
B.
$R_L \approx 2(\Delta L)$

C.
$R_L > 2(\Delta L)$

D.
$R_L > R_L$ (ABOVE)

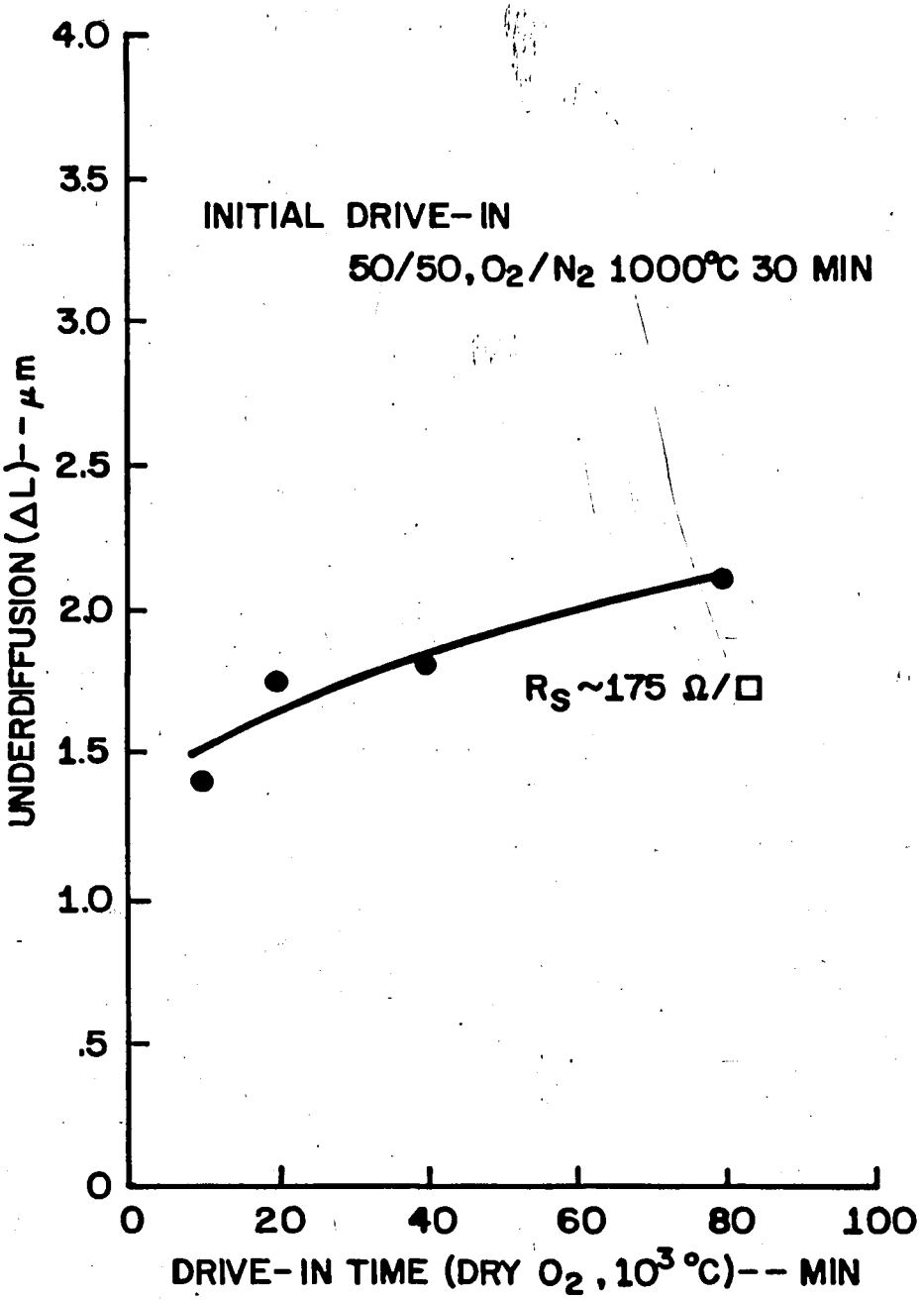
E.
$R_L > R_L$ (ABOVE)

FIGURE 5



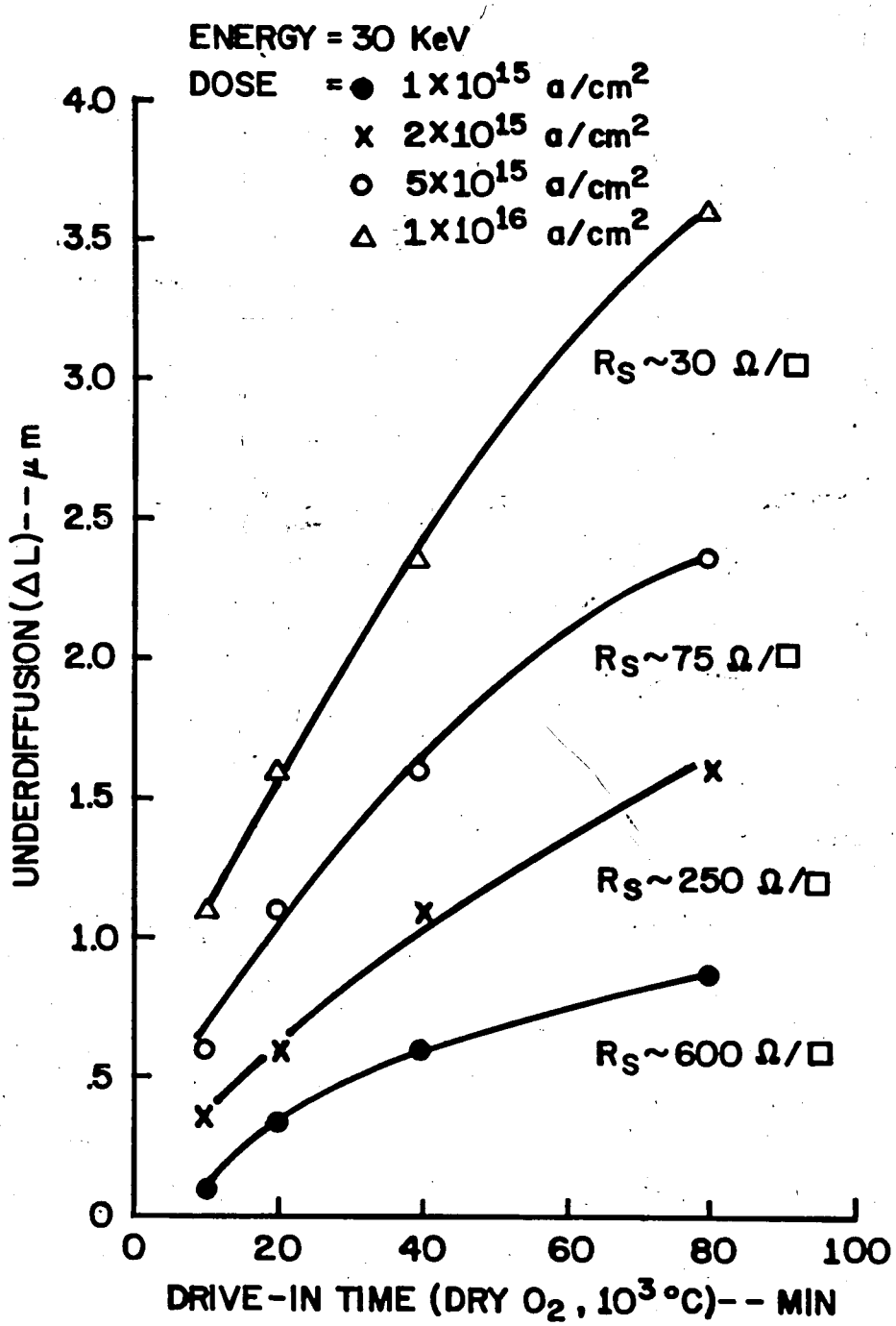
ARSENIC ION IMPLANT

FIGURE 6



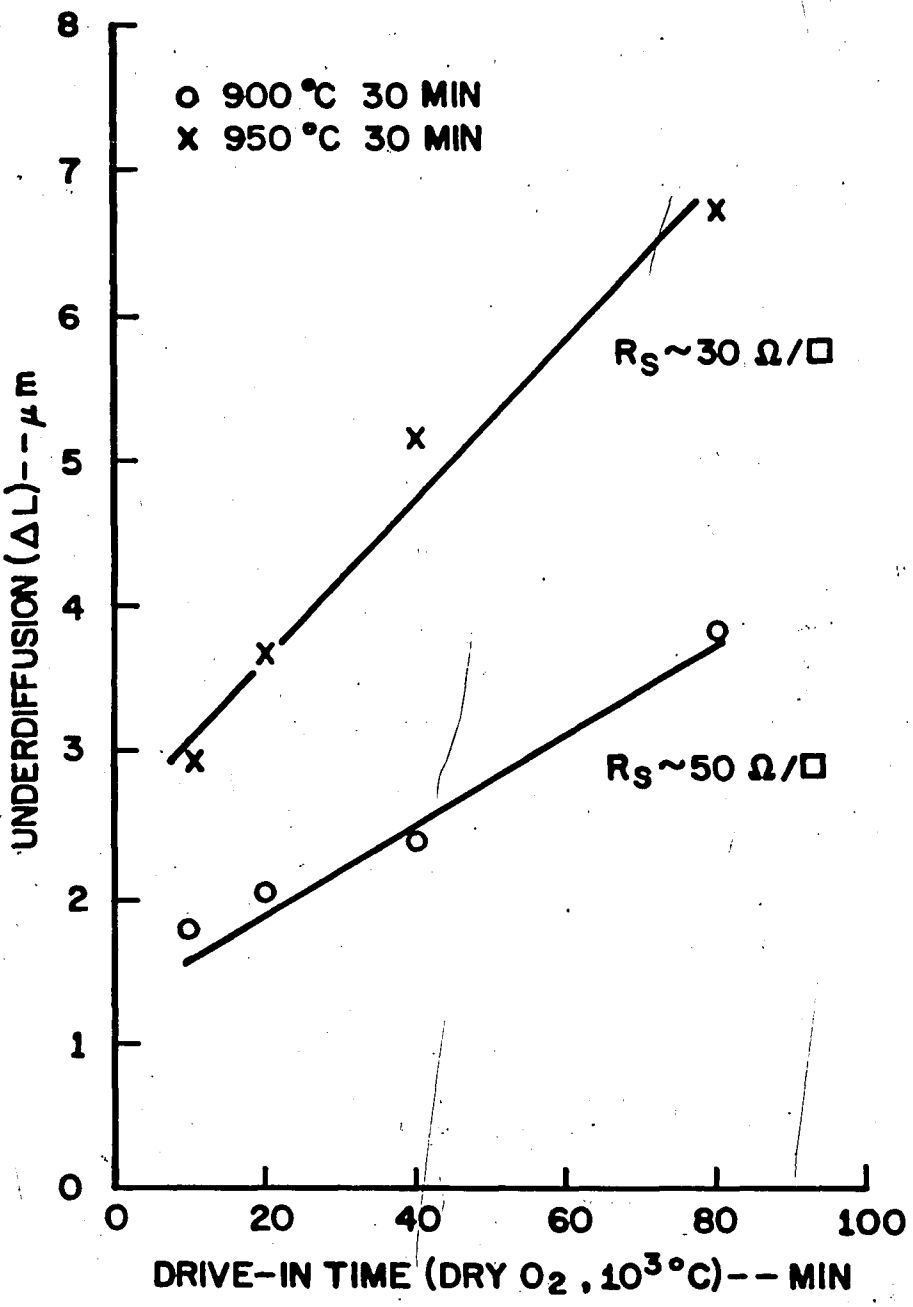
ARSENIC EMULSION BASE

FIGURE 7



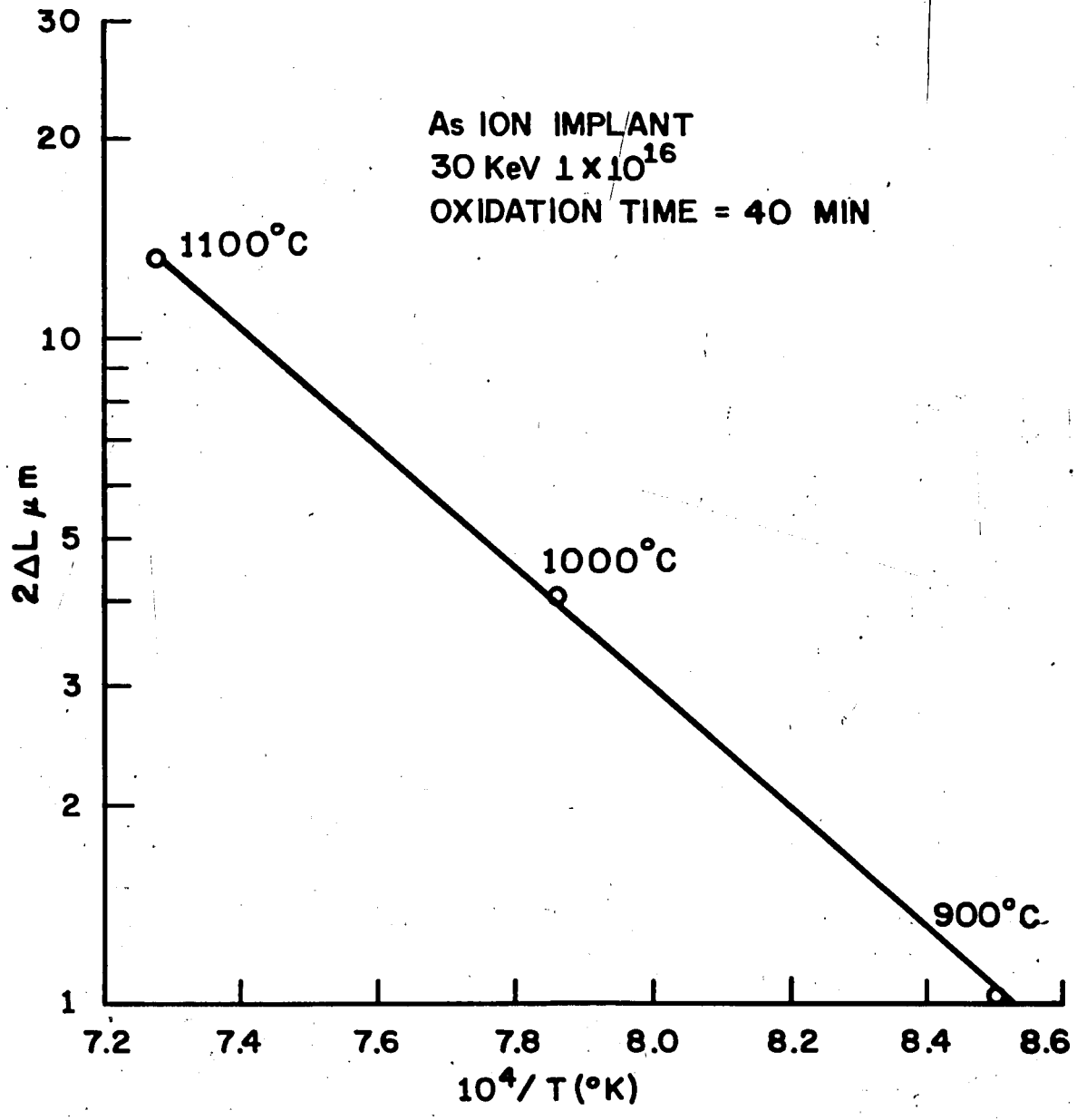
PHOSPHORUS ION IMPLANT

FIGURE 8



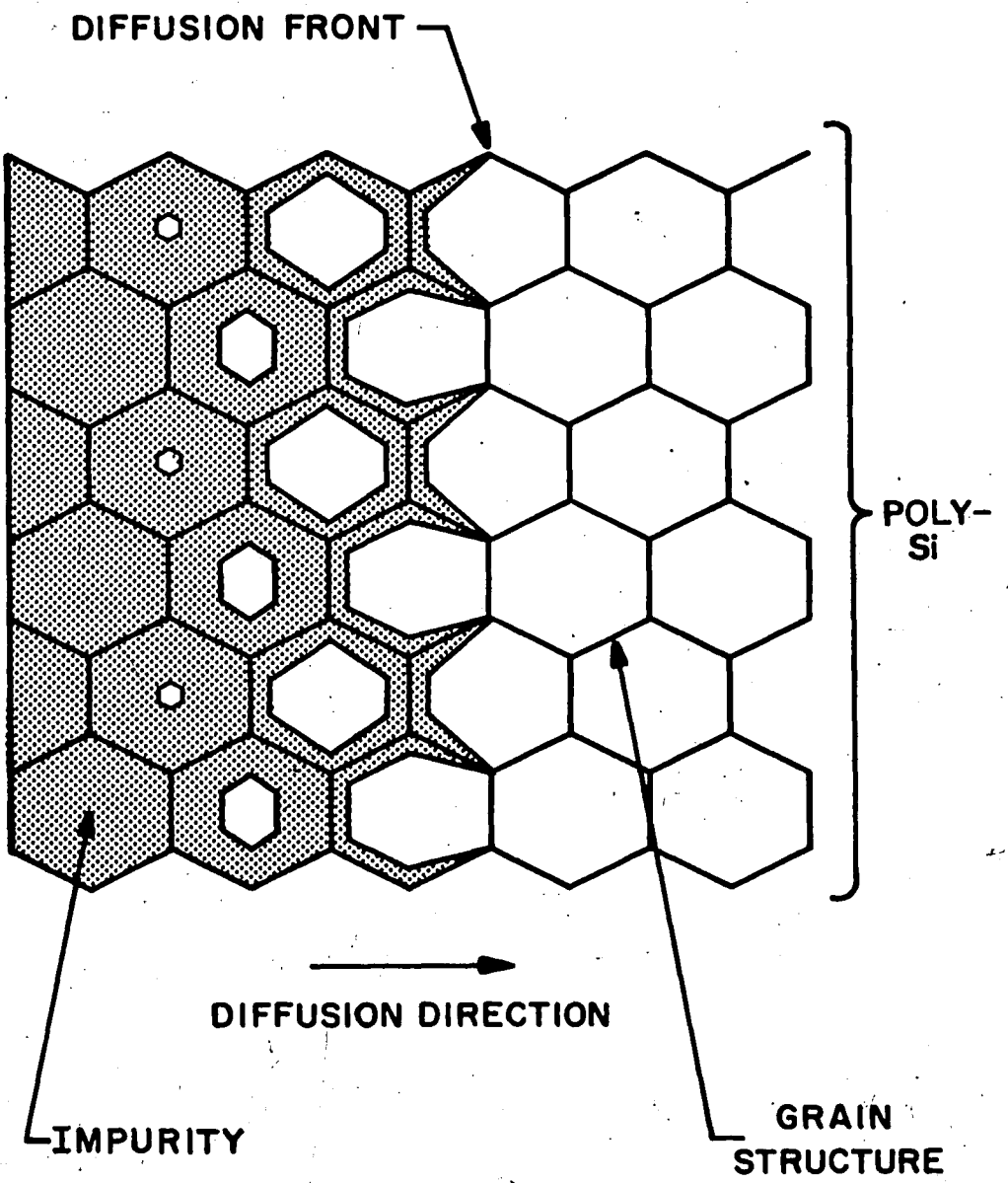
PHOSPHORUS PREDEPOSITION

FIGURE 9



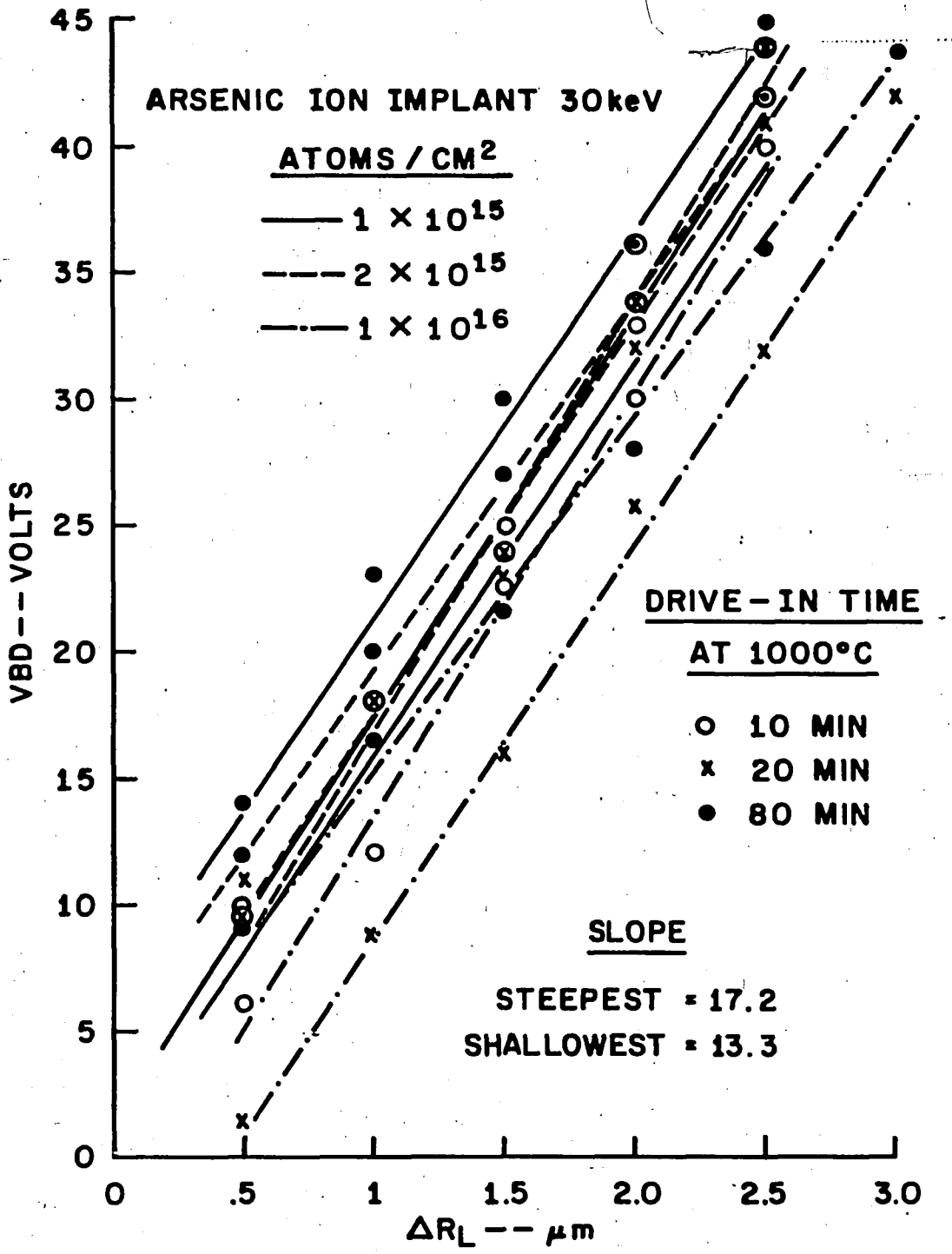
2ΔL VS TEMPERATURE^{-1}

FIGURE 10



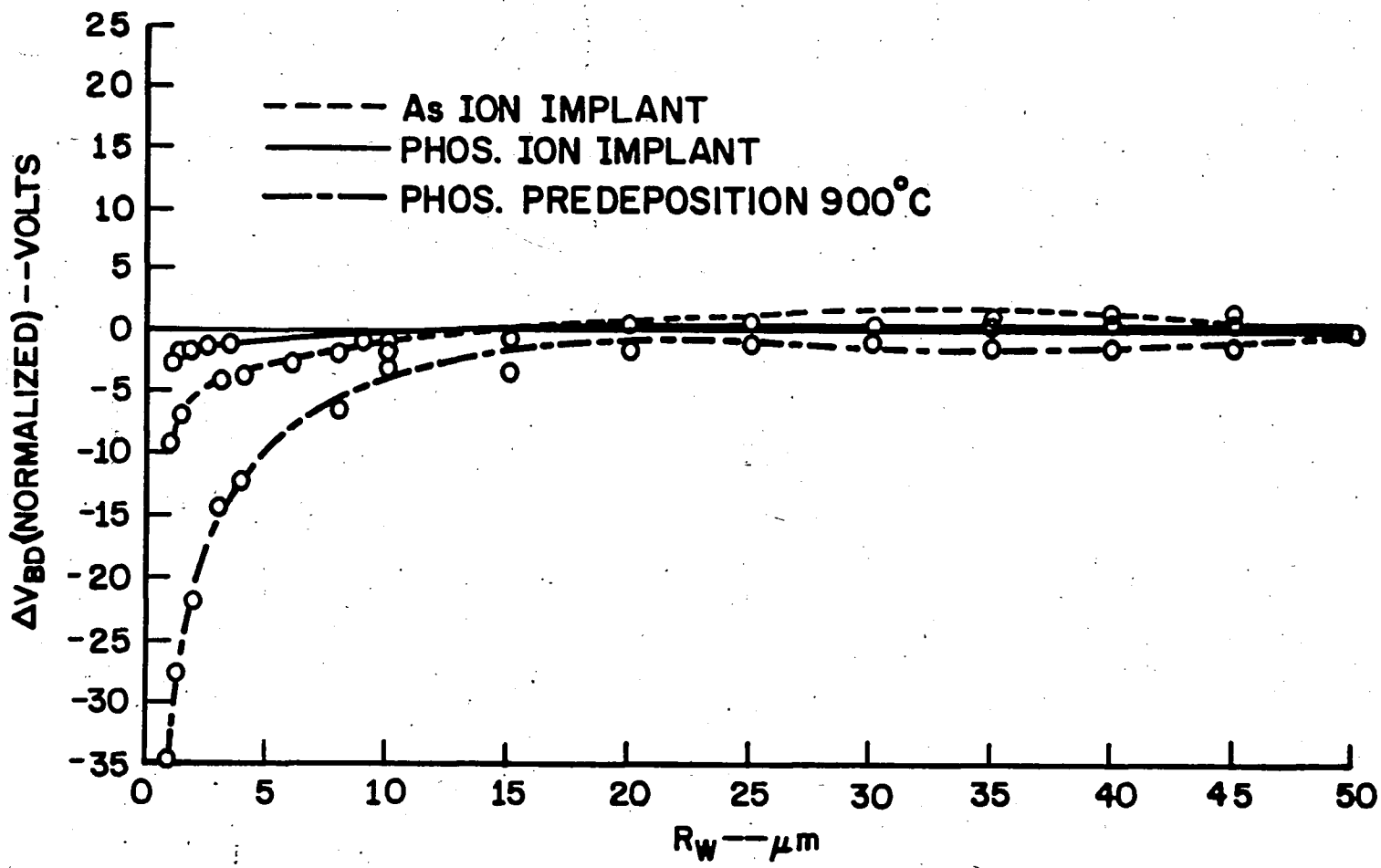
SYMBOLIC REPRESENTATION
OF IMPURITY DIFFUSION THROUGH POLY-Si

FIGURE 11



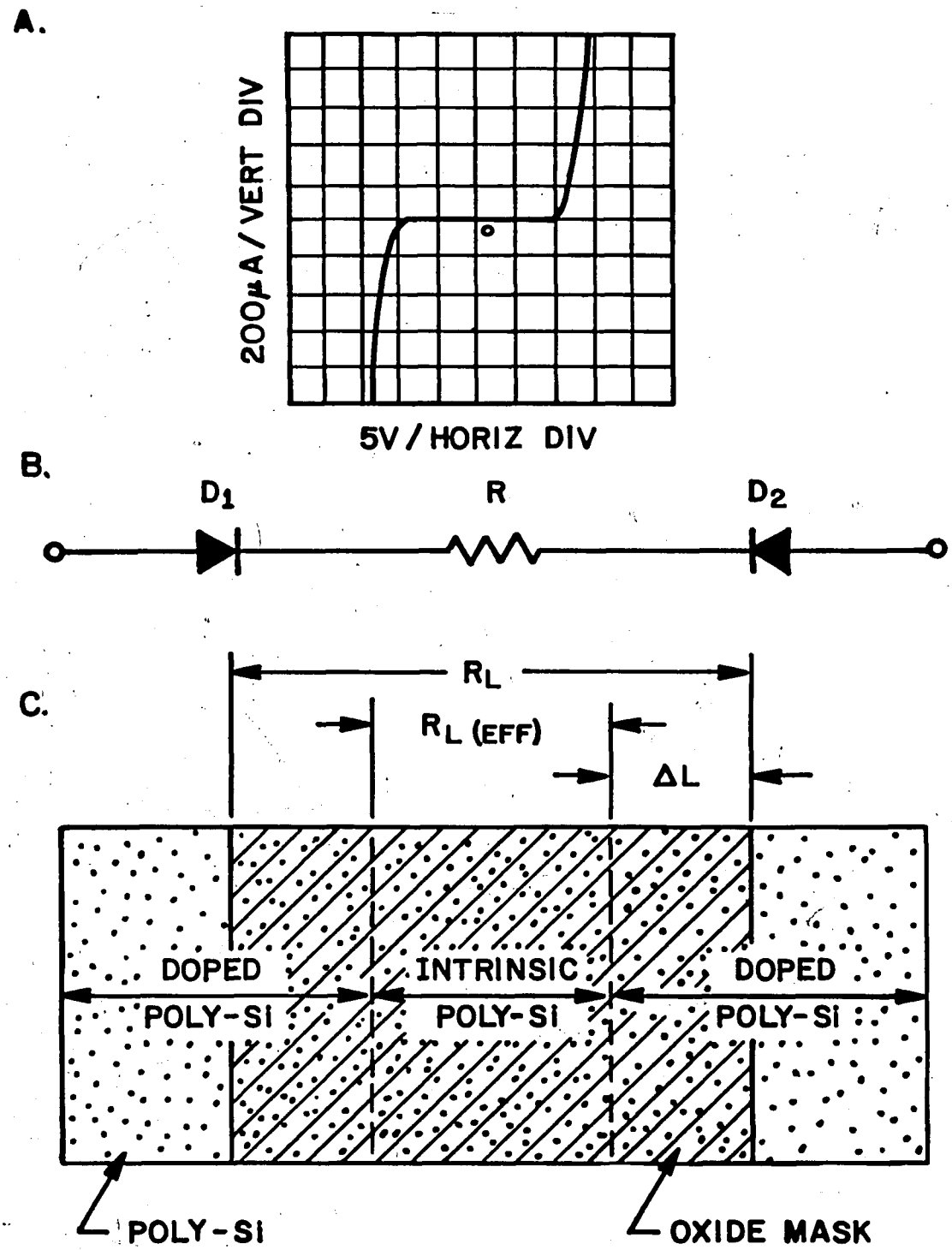
V_{BD} VS R_L

FIGURE 12



BREAKDOWN VOLTAGE DEPENDENCE ON RESISTOR WIDTH

FIGURE 13



A. I-V CURVE B. SCHEMATIC C. PHYSICAL MODEL

FIGURE 14

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APPENDIX 1

$$D = D_o \, e^{-E/kT}$$

$$2\Delta L \sim \sqrt{Dt}$$

for a given t:

$$\Delta L \sim \alpha \sqrt{D}$$

$$D^{1/2} = (D_o \, e^{-E/kT})^{1/2}$$

$$= D_o^{1/2} \, e^{-E/2kT}$$

$$1/2 \, \ell n \, D = 1/2 \, \ell n \, D_o - E/2kT$$

$$1/2 \log D = 1/2 \log D_o - E/2(2.3) \, k(1/T)$$

form:

$$y = b - m \, x$$

$$m = \text{slope} = \frac{\log 12 - \log 2}{(7.32-8.22)\,(10^{-4})} = 8.6 \;\; 4 \times 10^3$$

$$8.64 \times 10^3 = \frac{E}{4.6 \, k}$$

$$E = (8.64 \times 10^3)\,(4.6)\,(8.62 \times 10^{-5})$$

$$\therefore E = 3.4 \text{ eV}$$

VITA

Mr. Raymond H. Doklan was born in Quakertown, Pennsylvania on February 2, 1942, the son of Mr. and Mrs. Frank Doklan, Senior. He graduated from Bethlehem High School, Bethlehem, Pennsylvania in June, 1960. He served two years active duty in the United States Navy as an electronics technician stationed in Norfolk, Virginia. Following his honorable discharge from the Navy, he attended Pennsylvania State University Extension Center in Allentown, Pennsylvania where he earned an Associate Degree in Electrical Engineering. He graduated Magna Cum Laude with a Bachelor of Science Degree in Electrical Engineering from Lafayette College, Easton, Pennsylvania in June, 1972. He is a member of Eta Kappa Nu, Tau Beta Pi, and Phi Beta Kappa. He joined Bell Laboratories in June, 1964. Currently he is an Associate Member of the Technical Staff involved in process development for integrated circuits. He and his wife, the former Constance G. Vollman, and their children, Heather, Bradford, and Raymond C., reside in Whitehall, Pennsylvania.